IN THE CLAIMS

Please amend the claims as follows.

1. (Canceled)

2. (Canceled)

3. (Currently Amended) ~~The processor of claim 1~~ A processor comprising:

a mechanism to identify memory as secure memory accessible by secure processes, and to identify non-secure memory accessible by both secure and non-secure processes;

a security enforcement mechanism to allow page tables for the non-secure processes to be stored in secure memory; and

a translation look-aside buffer (TLB), wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process;

wherein the security enforcement mechanism includes page table walk hardware capable of walking page tables in secure memory in response to architecture events other than TLB misses caused by non-secure processes.

4. (Currently Amended) ~~The processor of claim 1~~ A processor comprising:

a mechanism to identify memory as secure memory accessible by secure processes, and to identify non-secure memory accessible by both secure and non-secure processes;

a security enforcement mechanism to allow page tables for the non-secure processes to be stored in secure memory; and

a translation look-aside buffer (TLB), wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a non-secure process;

wherein the security enforcement mechanism includes circuits to differentiate between program generated memory accesses and architecture generated memory accesses, and to block program generated memory access from accessing secure memory.

5. (Canceled)

6. (Currently Amended) The processor of claim ~~1~~ 4 further comprising virtual address translation hardware to perform virtual address translation for non-secure processes via page tables in secure memory.

7. (Canceled)

8. (Currently Amended) The processor of claim ~~1~~ 4 further comprising a control register to specify whether page tables for non-secure processes are kept in secure memory or non-secure memory.

9. (Currently Amended) The processor of claim ~~1~~ 4 further comprising page table walk hardware ~~capable of accessing~~ configured to access secure memory on behalf of non-secure processes.

10-23. (Canceled)

24. (Currently Amended) An electronic system comprising:

a plurality of antennas;

an amplifier coupled to at least one of the plurality of antennas to amplify communications signals;

a processor coupled to the amplifier; and

memory that can be partitioned by the processor into secure memory accessible by secure processes and non-secure memory accessible by secure or non-secure processes;

wherein the processor includes a security enforcement mechanism to allow page tables for non-secure processes to be stored in secure memory, and the processor includes a translation look-aside buffer (TLB), wherein the security enforcement mechanism allows a page table access in secure memory while the processor remains in a non-secure mode after a TLB miss in a

non-secure process[[.]], and wherein the security enforcement mechanism includes page table walk configured to walk page tables in secure memory in response architecture events other than TLB misses caused by non-secure processes.

25. (Canceled)

26. (Canceled)

27. (Currently Amended) A processor comprising:

secure memory accessible when the processor is in a privileged secure mode or a user secure mode;

non-secure memory accessible when the processor is in a privileged non-secure mode or a user non-secure mode; and

a security enforcement mechanism that allows access to page tables in secure memory when a translation look-aside buffer (TLB) miss occurs in the user non-secure mode, wherein the access to the page table occurs without the processor leaving the user non-secure mode[[.]], and wherein the security enforcement mechanism is configured to allow access to page tables in secure memory when a translation look-aside buffer (TLB) miss occurs in the privileged non-secure mode, wherein the access to the page table occurs without the processor leaving the privileged non-secure mode.

28. (Canceled)

29. (Previously Presented) The processor of claim 27 further comprising a memory management unit to access the page table while the processor remains in the user non-secure mode.

30. (New) The electronic system of claim 24 wherein the processor further includes a control register to specify whether page tables for non-secure processes are kept in secure memory or non-secure memory.

31. (New) The electronic system of claim 24 wherein the processor further includes page table walk hardware configured to access secure memory on behalf of non-secure processes.

32. (New) The processor of claim 27 further comprising a control register to specify whether page tables for non-secure processes are kept in secure memory or non-secure memory.

33. (New) The processor of claim 27 further comprising page table walk hardware configured to access secure memory on behalf of non-secure processes.

34. (New) A processor comprising:

secure memory accessible when the processor is in a privileged secure mode or a user secure mode;

non-secure memory accessible when the processor is in a privileged non-secure mode or a user non-secure mode; and

a security enforcement mechanism that allows access to page tables in secure memory when a translation look-aside buffer (TLB) miss occurs in the user non-secure mode, wherein the access to the page table occurs without the processor leaving the user non-secure mode and wherein the security enforcement mechanism includes circuits to differentiate between program generated memory accesses and architecture generated memory accesses, and to block program generated memory access from accessing secure memory when the processor is in the privileged non-secure mode or the user non-secure mode.

35. (New) The processor of claim 34 further comprising a control register to specify whether page tables for non-secure processes are kept in secure memory or non-secure memory.

36. (New) The processor of claim 34 further comprising page table walk hardware configured to access secure memory on behalf of non-secure processes.